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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/496,793	02/02/2000	Farooq Jabbar	60705-1210	6699

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EXAMINER

ODOM, CURTIS B

ART UNIT	PAPER NUMBER
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2634

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DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/496,793

Applicant(s)

JABBAR ET AL.

Examiner

Curtis B. Odom

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,2,7,8,13 and 21-24 is/are allowed.
- 6) ☒ Claim(s) 3-6,9-12,14-20 and 25-28 is/are rejected.
- 7) ☒ Claim(s) 29 and 30 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 February 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 7-12, 16-18, and 25-30 objected to because of the following informalities: The phrase “the cyclic prefix” is suggested to be changed to “a cyclic prefix”. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 3-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claims 3-6, claims 3 recites the limitation “detecting a phase error between a received pilot tone and a local oscillator signal; applying the phase error to the input of a phase locked-loop to generate a frequency correction signal;...” With regards to the specification, it is the understanding of the examiner that the input to the phase locked-loop is the received signal and that the phase error detection is performed inside the phase locked-loop. On page 20, line 14-page 21, line 19 of the

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specification, the applicant describes the operation of the phase locked-loop wherein a far-end signal is input into the phase locked loop, not a phase error signal. Fig. 7 illustrates the components of the phase locked-loop in which the oscillator signal is combined with the pilot tone to detect phase error. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the phase error is detected in the PLL and not applied to the input of the PLL.

4. Claims 11, 12, and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 11 recites the limitation "applying the estimated phase error to the input of a phase locked-loop to create a frequency correction signal;..." With regards to specification (page 20, line 14-page 21, line 19), the phase locked-loop of Fig. 7 is not capable of receiving a phase error signal. It is the understanding of the examiner that the input to the phase locked-loop is the received signal and that the phase error detection is performed inside the phase locked-loop.

5. Claims 19 and 20 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 19 recites the limitation "state machine in communication with the ADC configured to determine the phase offset on a pilot tone in a received signal segment; and a phase locked-loop in communication

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with the state machine configured to compensate for the phase offset...” With regards to specification (page 20, line 14-page 21, line 19), the phase locked-loop of Fig. 7 is not capable of receiving a phase offset signal. It is the understanding of the examiner that the input to the phase locked-loop is the received signal and that the phase error detection is performed inside the phase locked-loop.

6. Claims 25 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 25 recites the limitation “a phase locked-loop in communication with the ADC and DFT configured to receive the pilot tone phase error estimate...” With regards to specification (page 20, line 14-page 21, line 19), the phase locked-loop of Fig. 7 is not capable of receiving a phase error estimate. It is the understanding of the examiner that the input to the phase locked-loop is the received signal and that the phase error detection is performed inside the phase locked-loop.

7. Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 27 recites the limitation “means for detecting a phase error between a received pilot tone and a local oscillator signal; means for applying the phase error to a phase locked-loop to generate an output signal;...” With regards to the specification, it is the understanding of the examiner that the input to the phase locked-loop is the received signal and that the phase error detection is performed inside the phase

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locked-loop. On page 20, line 14-page 21, line 19 of the specification, the applicant describes the operation of the phase locked-loop wherein a far-end signal is input into the phase locked loop, not a phase error signal. Fig. 7 illustrates the components of the phase locked-loop in which in the oscillator signal is combined with the pilot tone to detect phase error. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the phase error is detected in the PLL and not applied to the input of the PLL.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Chun et al. (U.S. Patent No. 6, 101, 230).

Regarding claim 14, Chun et al. discloses a DSP (Fig. 1) configured to compensate for the offset is phase error on a received pilot tone by sending a signal to a phase-locked loop based upon the received signal segment in the DMT initialization sequence (column 1, line 52-column 2, line 66).

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10. Claims 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Spruyt et al. (U.S. Patent No. 6, 088, 386).

Regarding claim 16, Spruyt et al. discloses a DSP (Fig. 1) configured to detect and zero out a cyclic prefix from a received digital signal stream at an input to a phase locked loop when the cyclic prefix is present (column 6, lines 16-26).

Regarding claim 17, which inherits the limitations of claim 16, Spruyt et al. discloses the DSP is configured to perform a time-domain equalization on a received digital data stream and to create an input to a phase locked-loop when the cyclic prefix is zeroed out from the signal stream (column 8, lines 16-26).

Regarding claim 18, Spruyt et al. discloses a DSP configured to detect and remove the cyclic prefix from a received signal stream when the cyclic prefix is present, the digital signal processor further configured to first perform a time-domain equalization of the digital signal stream, then to perform a discrete Fourier transform (FFT) on the digital signal stream when the cyclic prefix is not present to create a phase error signal for application at the input to a phase locked-loop (column 8, lines 16-26).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chun et al. (U.S. Patent No. 6, 101, 230).

Regarding claim 15, which inherits the limitations of claim 14, Chun et al. further discloses the phase error compensation is accomplished with a phase detector (Fig. 1, block 16, column 4, lines 6-62). Chun et al. does not disclose the phase error compensation is accomplished by a state machine. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that since the state machine is also used for phase error compensation that it could have been implemented in place of the phase detector. Thus, a state machine used to compensate for phase error is deemed a design choice and does not constitute patentability.

13. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spruyt et al. (U.S. Patent No. 6, 088, 386) in view of Chun et al. (U.S. Patent No. 6, 101, 230).

Regarding claim 9, Aslanis et al. discloses a method for timing recovery at the receiver in a DMT communications system (Fig. 1) comprising:

receiving (Fig. 1, column 3, lines 26-28) a standard pilot tone generated and transmitted by an associated far-end transmission unit along with other signal streams at a particular receiver;

converting (Fig. 1, AD, column 8, lines 12-33) the plurality of received signals through an ADC to create a digital signal stream;

detecting (Fig. 1, CPER, column 8, lines 12-33) the cyclic prefix in the received digital signal stream;

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performing (Fig. 1, TEQ, column 8, lines 12-33) a time-domain equalization on the received signal stream;

removing (Fig. 1, CPER, column 8, lines 12-33) the cyclic prefix portion of the equalized digital signal stream from the input to a PLL to create a frequency correction signal (Fig. 1, PLL column 5, lines 25-66), wherein the PLL creates a frequency correction signal; and

However, Spruyt et al. does not disclose using the frequency correction signal to modify the ADC sampling time.

Chun et al. discloses a PLL in a DMT communication system which creates a frequency correction signal using a pilot tone phase which is applied to the ADC to modify the ADC sampling time (Fig. 1, block 16, column 3, line 31-column 4, line 62). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the device of Spruyt et al. with the PLL of Chun et al. to control the clock of Spruyt et al. to allow synchronization of the sampling clocks of the transmitter and the receiver by being able to tune the sampling clock of the receiver which would allow for a more accurate and efficient recovery of transmitted data in the receiver.

Regarding claim 10, which inherits the limitations of claim 9, Spruyt et al. discloses synchronizing a DAC in the transmitting path by using a sampling clock from the ADC (Fig. 1, column 6, lines 50-54).

Allowable Subject Matter

14. Claims 1, 2, 7, 8, 13, 21-24, 29 and 30 are allowable over prior art (if above objections are overcome) because related references do not disclose generating signal segments REVERB and SEGUE using an initial pattern that minimizes pilot tone phase offsets and a symbol synchronizer for zeroing out a signal stream when a cyclic prefix is present in the signal stream to create a frequency correction signal.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Verbueken (U. S. Patent No. 5, 867, 528) also discloses a method of timing recovery using a PLL in a DMT system.


16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 703-305-4097. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 709-872-9306 for regular communications and 703-872-9306 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Curtis Odom
February 6, 2004



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